10nm CPI Study for Fine Pitch Flip Chip Attach Process and Substrate

by

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Abstract

The rapid growth rate of advance technology developments in the semiconductor industry is driving the evolution in emerging markets to satisfy the increasing requirements of higher performance, higher bandwidth and lower power consumption as well as multiple functions in portable and mobile devices. Electronic devices have evolved from a simple communication device to a complicated and highly integrated system with multiple functions required. Moving forward with this trend, packaging semiconductor devices for mobile electronics is more challenging than ever before, pushing smaller form factor package designs and developments in emerging markets. To meet these demands, developments in advanced silicon (Si) nodes, finer bump pitch attach processes as well as finer line width and spacing (LW/LS) substrate manufacturing has become a hot topic in the industry. For example, look at the Si node development status. While 20/16/14nm technology is widely utilized today in mobile applications to pursue the die size reduction, efficiency enhancement and lower power consumption, 10nm technology is receiving increasing attention. Based on the requirements and evolution of mobile applications, package types have migrated from wire bond packaging to flip chip chip scale package (fcCSP) to deliver cleaner power to the device, provide higher input/output (I/O) to accommodate the volume of high speed consumer devices and still satisfy all other requirements without compromising reliability and/or cost. In order to achieve high I/O solutions, finer flip chip bump pitch as well as finer line width and spacing are becoming the attractive solution to meet this target. Flip chip interconnect with copper (Cu) pillar bond-on-lead (BOL) and enhanced processes (fcCuBE®) can deliver a high performance packaging solution with a cost effective mass reflow (MR) manufacturing process. The robust flip chip bump process with copper pillar technology in fcCuBE® has been widely adopted to achieve bump pitch reduction, performance improvement and Si node reduction. In order to realize the chip-package interaction (CPI) in a fcCSP with 10nm backend process daisy-chain die and Cu pillar BOL architecture, the cost effective solution of mass reflow flip chip attach process with 90µm and 60µm bump pitch and a 2-layer embedded trace substrate (ETS) is evaluated. The quick temperature cycling (QTC) test is performed to realize the 10nm extremely low-k (ELK) performance in a fcCSP. Through these results, the significant factors to impact ELK performance can be delivered to enhance the yield in the chip attach process. It is believed that this successful data can help guarantee the 10nm flip chip assembly yield without ELK damage issues in the future.

Key words: 10nm Si node, flip chip package, chip-package interaction, copper pillar bump, embedded trace substrate, quick temperature cycling test,

1. Introduction

Emerging markets are always driving demand for higher performance, higher bandwidth, lower power consumption as well as increasing functionality in mobile applications. Packaging technology has become more challenging and complicated than ever before, driving advanced silicon (Si) nodes, finer bump pitch as well as finer line width and spacing substrate manufacturing capabilities to satisfy the increasing requirements in the semiconductor industry. As increasing input/output (I/O) counts in a package are needed in mobile devices, packaging solutions are migrating from traditional wire bond packages to flip chip interconnect to meet these requirements. Flip chip chip scale package (fcCSP) is viewed as an attractive solution for complicated and highly integrated systems with multiple functions and heterogeneous mobile applications [1-5]. Although emerging markets are driving advanced technologies in high performance mobile devices, assembly cost

is still the major issue to be addressed. As the substrate cost is always the significant factor in a flip chip package, flip chip assembly with a low cost substrate has become a hot topic in the industry. In the flip chip assembly process, substrate technology has been moving from traditional bond-on-capture (BOC) pad with cored substrate to bond-on-lead (BOL) with coreless substrate in recent years. Embedded trace substrate (ETS) has been widely adopted for low cost requirements. In addition, flip chip interconnect with copper (Cu) pillar BOL and enhanced processes (fcCuBE®) can help to deliver a high performance packaging solution with a cost effective mass reflow (MR) manufacturing process [6-7]. By using the above technologies, it has been proven that not only can it meet the packaging cost reduction, but it can also achieve a thin flip chip package profile.

Due to the fast growth in emerging markets for mobile applications, advanced Si node technology development for mobile applications is moving to 10nm technology (and below) and pursuing the die size reduction, efficiency enhancement and lower power consumption now. For the sake of realizing the 10nm extremely low-k (ELK) performance in a flip chip package, the 10nm chip-package interaction (CPI) study in a 15x15mm fcCSP with finer Cu pillar bump pitch and a 2-layer embedded trace substrate (ETS) with finer line width/spacing (LW/LS) design is illustrated in this paper. The utilizations of 90µm and 60µm bump pitch with escaped trace and mass reflow flip chip attach process are estimated. The quick temperature cycling (QTC) test with temperature range of -40 C to 60 C is performed to realize the ELK performance in a 10nm flip chip package. In addition, the comparison of different UBM sizes and reflow profiles has been also studied. With the evaluated results, not only the significant factors that impact ELK performance can be obtained, but the optimized reflow profile can also be established to enhance the yield in flip chip attach processes. It is believed that the illustrated robust flip chip attach processes examined in this paper can guarantee 10nm fine bump pitch flip chip assembly yield with less ELK damage risk in the future.

2. CPI Study in 90µm Bump Pitch fcCSP

In order to study the ELK performance in 10nm Si node technology, a 15x15mm fcCSP with 10nm ELK backend process daisy-chain die is used as the test vehicle in this section. Die size of ~135mm^2 and die thickness of 200µm is evaluated. The fine Cu pillar bump pitch of 90µm and bump height of 58µm is utilized in this fcCSP. The cost effective solution of the MR flip chip attach process is adopted for Cu pillar bump attach on a low cost 2-layer ETS with finer LW/LS and escaped trace design. The 80µm prepreg thickness is utilized in a 2-layer ETS with total substrate thickness of 150µm. A CuOSP surface treatment process is used on the bottom ball pads with lead-free ball and 0.4mm ball pitch options. The overall maximum package thickness is set to be less than 0.9mm

Figure 1 shows the process flow in a 10nm fcCSP with MR flip chip attach process. Two kinds of prepreg materials in a 2-layer ETS are evaluated in the flip chip assembly process, with material properties listed in Table 1. The QTC test (after flip chip attach process and without proceeding molded underfill (MUF) process) with temperature change from -40 C to 60 C and ramp-up/ramp-down rate of 30 C/min as well as dwell time of ~5 minutes is performed to detect if there is any white bump phenomenon in a fcCSP through C-Mode Scanning Acoustic Microscopy (C-SAM) inspection. Table 2 listed the QTC evaluation results from time zero status (T0) to QTC 60 times (60x) in 3 different legs. All 3 legs passed QTC 60x without any failure with C-SAM inspection. Figure 2 shows the C-SAM results of Leg#1 from T0 to QTC60x and no observed white bump phenomenon in a 10nm fcCSP. To further check if there is any failure after QTC60x, the Scanning Electron Microscope (SEM) cross-sectional views of Leg#2 and Leg#3 are also illustrated in Figure 3, which clearly show that there is no abnormality of ELK failure in these legs.

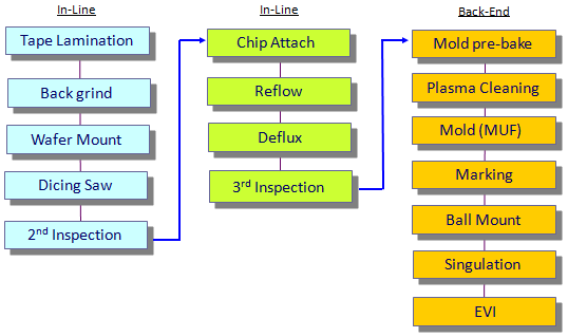
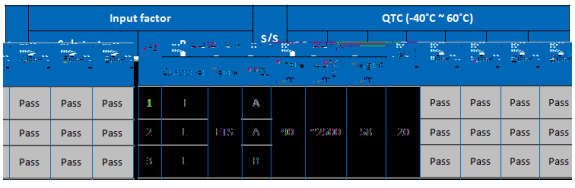


Figure 1: Flip chip package (fcCSP) with MUF process flow.

Table 1: Prepreg material properties.

Prepreg Material Properties		PPG-A	PPG-B
Tg (°C)	DMA	300	255
	TMA	270	230
CTE - XY (ppm/°C)	Below Tg (α1)	5	12
	Above Tg (α2)	2	5
CTE – Z (ppm/°C)	Below Tg (α1)	21	28
	Above Tg (α2)	100	165
Young's Modulus (GPa)	RT(25°C)	24	18
	PT(260°C)	15	11

Table 2: QTC results for 90µm bump pitch evaluation.



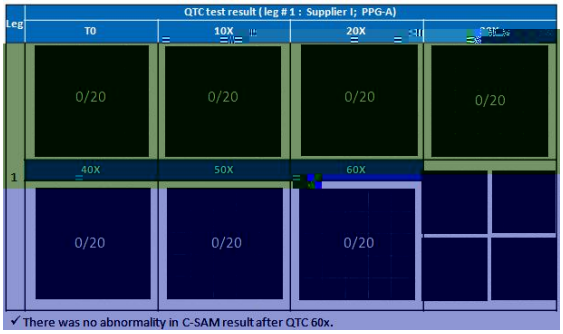


Figure 2:QTC results through C-SAM inspection in Leg#1.

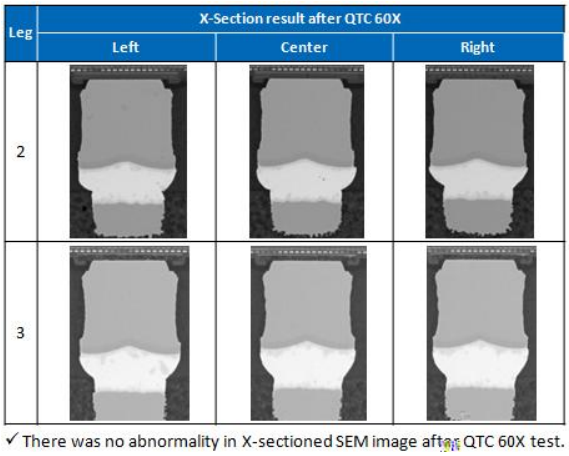


Figure 3: SEM cross-sectional images in Leg#2 and 3 after QTC60x.

Since package warpage and coplanarity behavior are typically requested to meet Surface Mount Technology (SMT) processes without any issue, maximum warpage of 80µm at high temperature (260 C) and maximum coplanarity of 80µm specifications are always required in flip chip technology [5, 8]. Figure 4 illustrates the warpage behavior distribution at every temperature read points in this fcCSP, which clearly indicates that all three legs can meet the package warpage specification of less than 80µm at every temperature read point and the maximum warpage can be reduced to less than 60µm. In addition, through the coplanarity assessment, it is found that all three legs can meet the requirement and with the use of PPG-A will have better coplanarity control, which is shown in Figure 5.

As the flip chip bump pitch become finer, solder bridge risk during the MR chip attach process is always the key issue to be overcome. In order to understand if there is any solder bridge phenomenon occurring during the flip chip assembly process, the confirmation build of 1000 units sample size (with dummy dies) with Leg#2 condition is estimated to evalute the package assembly yield. Figure 6 illustrates the assembly yield result by using X-ray/External Visual Inspection (EVI), which indicates that no solder bridge was observed during the fcCSP assembly build. Moreover, this fcCSP with 10nm ELK backend process daisy-chain die also passed long term reliability tests such as pre-condition of moisture sensitivity level (MSL2aA and MSL3) as well as unbiased highly accelerated stress test (uHAST) of 96 hours and thermal cycling test condition B (TCB) of 1000 cycles without any defect observed. The package reliability results with Leg#2 and 3 assessments are illustrated in Figure 7 based on utilizing Through Scanning Acoustic Microscopy (T-SAM) inspection. The result shows that the illustrated robust flip chip attach processes examined in this study can guarantee 90µm bump pitch fcCSP assembly without any yield loss as well as any risk of solder bridge and ELK damage.

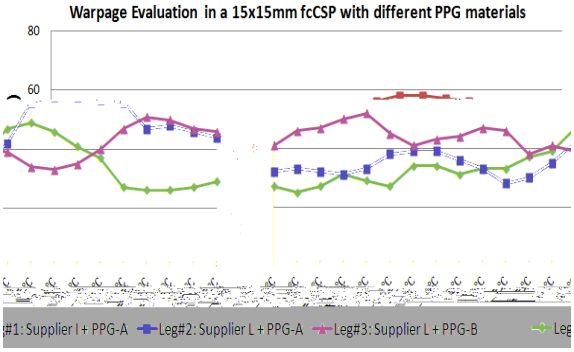


Figure 4: Warpage behaviors in a fcCSP with 2L ETS and different prepreg materials (S/S:10ea in each leg).

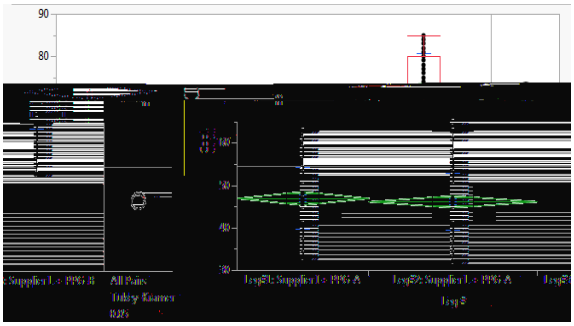
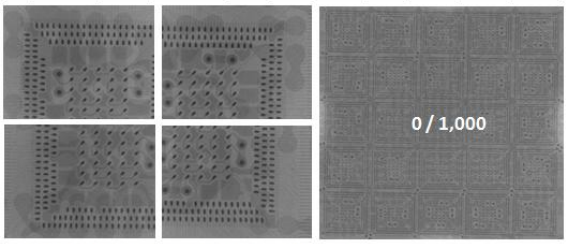


Figure 5: Coplanarity behaviors in a fcCSP with 2L ETS and different prepreg materials (S/S: 100ea in each leg).

Leg	Input factor						S/S (ea)	Solder Bridge (X-ray)	EVI reject	Yield
	Substrate			Bump						
	Tech.	Supplier	PPG	Pitch (µm)	UBM (µm²)	Height (µm)				
2	ETS	L	PPG-A	90	~2500	58	1,000	0/1,000	0/1,000	100%



✓ Solder bridge was not found at 100% x-ray inspection.

Figure 6: Assembly yield confirmation builds result.

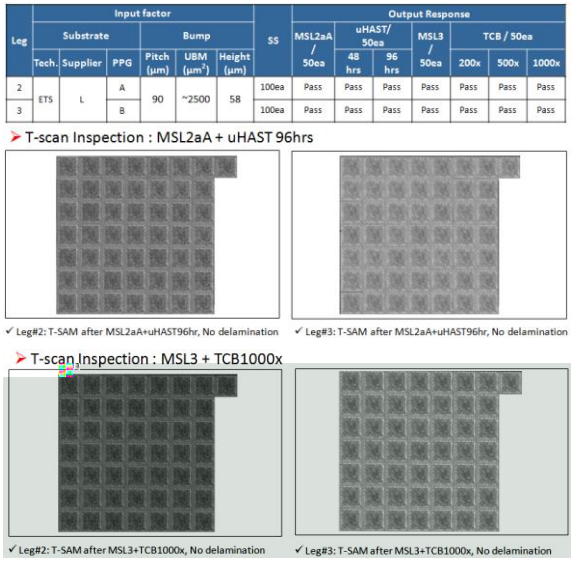


Figure 7: Long term package reliability result in 10nm fcCSP with 90μm bump pitch.

3. CPI Study in 60μm Bump Pitch fcCSP

In this section, the QTC test for 10nm ELK backend process daisy-chain die of ~135mm^2 die size in a 15x15mm fcCSP and a 2-layer ETS substrate (with 80μm prepreg thickness) are performed. The Cu pillar bump technology with fine bump pitch of 60μm with escaped trace and bump height of 55μm is utilized. In order to study the die thickness effect on 10nm ELK performance, die thickness of 65μm and 200μm with Cu pillar bump structure of ~1500μm^2 UBM is estimated in the QTC test. The fcCSP is with POR chip attach mass reflow process, which is also utilized in 90μm bump pitch evaluations. Through the QTC result that illustrated in Table 3, it is found that all legs failed and can t pass QTC60x specification by using current POR chip attach mass reflow profile. This result shows that the ELK performance is significantly impacted with the design of smaller Cu pillar bump pitch and smaller UBM size. In addition, the ELK performance in fcCSP with 65μm die thickness is illustrated to be better than that with 200μm die thickness. Therefore, the utilization of thinner die thickness is proven to have better ELK performance in QTC evaluations. Moreover, it is also shown that prepreg materials are not the critical factor to impact ELK performance in this 60μm bump pitch QTC estimations.

Table 3: QTC results for 60μm bump pitch evaluation with POR reflow profile.

Leg	Input factor							Die T (μm)	S/S	QTC (-40°C ~ 60°C)						
	Substrate			Reflow	Bump					0x	10x	20x	30x	40x	50x	60x
	Supplier	Tech.	PPG		Pitch (μm)	UBM (μm²)	Height (μm)									
A-1	S	ETS	A	POR	60	~1500	55	65	20	0/20	8/20	X	X	X	X	X
A-2			B					65		0/20	7/20	X	X	X	X	X
A-3			A					200		20/20	X	X	X	X	X	X
A-4			B					200		20/20	X	X	X	X	X	X

Since the larger UBM size is proven to improve ELK performance [9-10] and the reflow profile is also the critical factor to influence 10nm ELK performance with 60μm bump pitch technology, Table 4 illustrates the QTC result by adopting 150μm die thickness and larger UBM size of ~2000μm^2 with different polyimide layer opening (PIO) size as well as a modified reflow profile (MOD) in flip chip assembly process. The major difference of POR and MOD chip attach reflow profile is the cooling rate parameter. The MOD reflow profile is using a lower cooling rate when the temperature is below 220 C as compared to POR reflow profile. Table 4 clearly shows that the ELK performance significantly improved and can pass QTC30x without any failure by utilizing MOD reflow profile but still observe the white bump phenomenon and failure in QTC40x. The C-SAM results of Leg#B-1 and B-2 from T0 to QTC40x are illustrated in Figure 8. To further confirm the failure mode of both legs after QTC40x, the corresponding SEM cross-sectional images are shown in Figure 9. It is indicated that the ELK delamination was found at white bump position (shown in Figure 8) after QTC40x.

Table 4: QTC results for 60μm bump pitch evaluation with modified reflow profile.

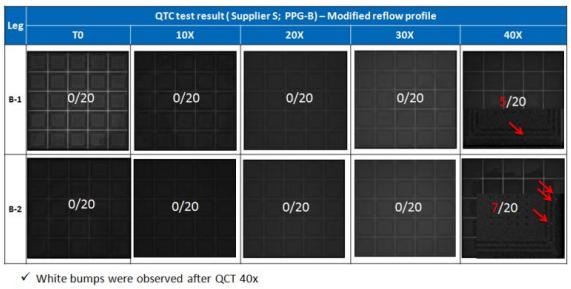


Figure 8: QTC results through C-SAM inspection in Leg#B-1 and B-2 (with modified reflow profile).

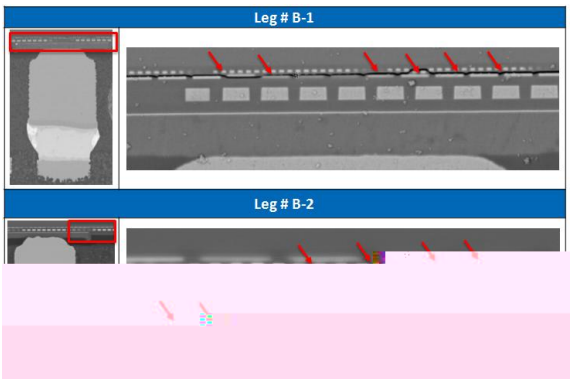


Figure 9: SEM cross-sectional images in Leg#B-1 and B-2 after QTC40x.

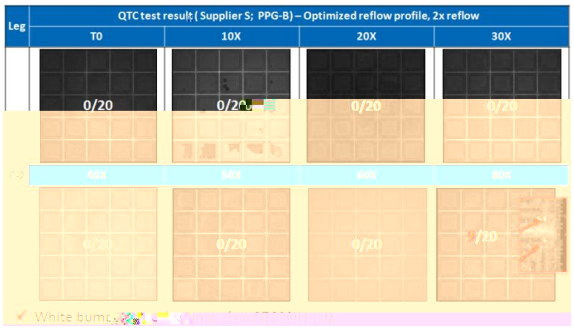
For the purpose of improving ELK performance to pass up to QTC60x in a 10nm fcCSP with 60μm bump pitch, an optimized flip chip attach

reflow profile (OPT) is established. Table 5 shows the corresponding QTC result in a 10nm fcCSP with 200µm die thickness. As shown on Table 5, it is found that with the optimized chip attach reflow profile (one-time reflow process), the QTC result can be improved to QTC100x without any failure. The white bump phenomenon is observed when QTC test extends to 150x, which C-SAM result is illustrated in Figure 10(a), Leg#C-1. Furthermore, the server condition of two-times flip chip attach reflow process is also estimated with OPT reflow profile in Leg#C-2, which illustrates that it can pass QTC60x without any ELK failure as well. Figure 10(b) shows the C-SAM result when two-times flip chip attach reflow process is performed and it is indicated that the white bump phenomenon was observed after QTC80x. The failure images of both legs through SEM are shown in Figure 11, which clearly indicates the ELK delamination occurs in the white bump area. Therefore, it is believed that the optimized robust flip chip attach reflow profile established in this section can reduce the risk of ELK damage in the 10nm fcCSP assembly with 60µm copper pillar bump pitch technology.

Table 5: QTC results for 60µm bump pitch evaluation with optimized reflow profile.

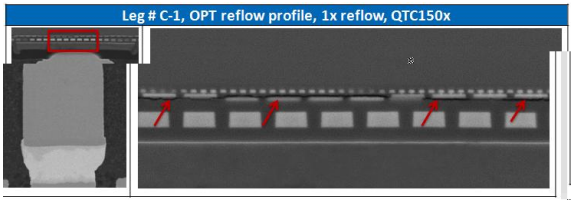
Leg	Input factor									QTC (-40°C ~ 60°C)								
	Substrate			Reflow	Reflow Times	Bump			Die T (µm)	S/S	0x	10x	20x	30x	40x	50x	60x	80x	100x
	Supplier	Tech.	PPG			Pitch (µm)	UBM (µm²)	Height (µm)											
C-1	S	ETS	B	OPT	1x	60	~2000	55	200	25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25
C-2					2x					20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	0/20	x

(a) with one-time reflow

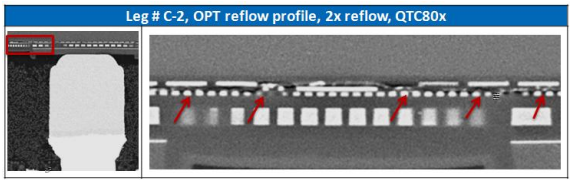


(b) with two-times reflow

Figure 10: QTC results through C-SAM inspection in Leg#C-1 and C-2 (with optimized reflow profile).



(a) Leg#C-1 after QTC150x;



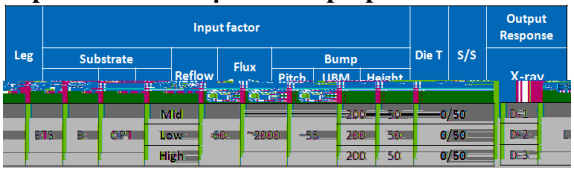
(b) Leg#C-2 after QTC80x

Figure 11: SEM cross-sectional images in Leg#C-1 and C-2 (with optimized reflow profile).

As the flip chip bump pitch is reduced to 60µm, the risk of solder bridge during the MR chip attach process will be more challenging, expecially when escaped trace design in the substrate. For the purpose of realizing if solder bridge phenomenon exist to cause short issue in this fcCSP, the corner study for different flux cavities during MR chip attach process is estimated. Table 6 illustrates the evaluation result for short confirmation and shows that no bump to trace short has been observed through X-ray insection. Figure 12 illustrates the result of die peel test, which shows the good bump joints after MR chip attach process in this confirmation build for 60µm bump pitch evaluation.

Figure 13 illustrates the warpage behavior distribution at every temperature read point in the 10nm fcCSP with 60µm bump. In this figure, the corresponding warpage distribution is well within the specification. Moreover, the long term reliability tests of MSL3 pre-condition with uHAST 96 hours, TCB 1000 cycles and HTST 1000 hours are also performed to demostrate package reliabilty, as shown in Figure 14. It can be concluded that the 10nm fcCSP with 60µm bump pitch passes all reliabilty test items without any defect observed through T-SAM inspection. Hence, it is believed that the optimized flip chip attach process and methodology examined in this section can guarantee the illustrated 10nm fcCSP (with 60µm bump pitch and escaped trace in a 2-layer ETS) assembly yield with less ELK damage risk.

Table 6: Confirmation results for short inspection in 60µm bump pitch evaluation



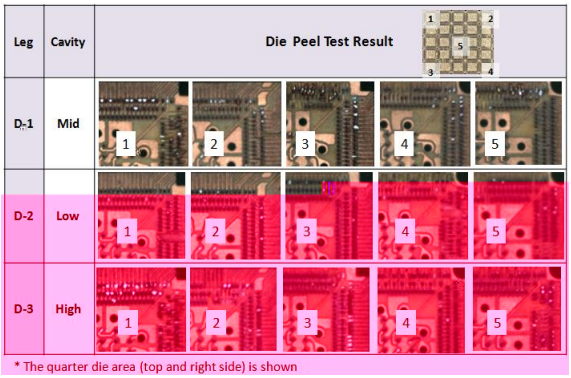


Figure 12: Result of bump joints inspection for 60µm bump pitch evaluation in die peel test.

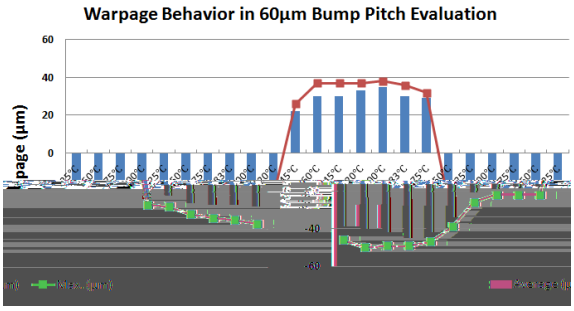


Figure 13: Warpage behaviors in a fcCSP with 60µm bump pitch (S/S:10ea in each leg)

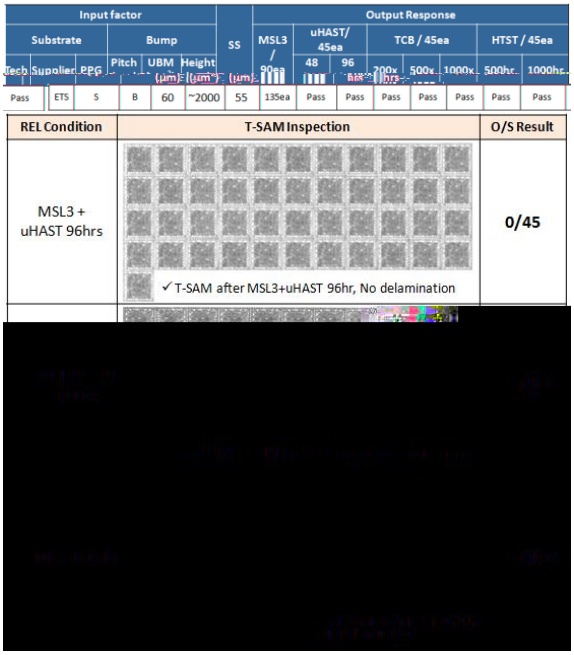


Figure 14: SEM Long term package reliability result in 10nm fcCSP with 60µm bump pitch.

4. Conclusions

This paper reports the 10nm CPI study of a 15x15mm fcCSP with finer copper pillar bump pitch and a 2-layer ETS with fine LW/LS and escaped trace design. A cost effective solution of mass reflow flip chip attach is performed in the fcCSP assembly process. The QTC test with temperature range of -40 C to 60 C is evaluated to confirm if there is any white bump phenomenon in a 10nm fcCSP. In order to deliver the reliable flip chip attach process in 10nm fcCSP, a comparison of different UBM sizes and reflow profiles effects has been also studied. With the evaluated results, the optimized reflow profile can be established to enhance the yield in chip attach process and the significant factors to impact ELK performance can be obtained as well. For the sake of estimating good bump joints by using established MR reflow profile in both 90µm and 60µm bump pitch evalutions, the confirmation build with dummy die is estimated and no bump to trace short issue is been observed. In addition, warpage/coplanarity assessments as well as long term reliability tests are also illustrated to show this fcCSP structure can not only meet the warpage/coplanarity but can also pass package reliability test without any defect observed. Through this study, it can help guarantee the 10nm flip chip assembly yield without ELK damage issues in the future.

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